INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional)	Application Number
BUR920030168 (17124)	10/707071
Applicant(s) Darren L. Anand, et al.	
Filing Date 11-19-03	**Group Art Unit**

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
/JK/		JP7078495	20/3/95	Japan	X	X		
/JK/		JP2002243801	28/08/02	Japan	X	X		
/JK/		JP2002298598A	11/10/02	Japan	X	X		

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

/JK/		International Test Conference, 1998 Proceedings, "Semiconductor Manufacturing Process Monitoring using Built-In Self-Test for Embedded Memories", Ivo Schanstra, Dharmajaya Lukita, Ad J. van de Goor, Kees Veelenturf, Paul J. van Winjnen, pp. 872-881

EXAMINER	DATE CONSIDERED
/James Kerveros/	03/20/2007

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

11/19/2003

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS

Application Number : 10/707,071

Confirmation Number:

First Named Applicant: Darren Anand

Attorney Docket Number: BUR920030168US1

Art Unit: 2138

Examiner: JAMES C. KERVEROS

Search string: (4876685 or 5936876 or 6185709 or 6509766 or 0084387).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
/JK/	1	4876685	1989-10-24	Rich			
	2	5936876	1999-08-10	Sugasawara			
	3	6185709	2001-02-06	Dreibelbis et al			
	4	6509766	2003-01-21	Pomichter et al			
	5	0084387	2003-05-01	Rooney et al			

Signature

Examiner Name	Date
/James Kerveros/	03/20/2007